REMARKS

The Examiner is thanked for the thorough examination of the present application. In view of the arguments presented in detail below, it is submitted that all of the claims are patentable.

I. The Claimed Invention

The present invention is directed to a method of transmitting data between two devices via a clock line and at least one data line, the clock line being maintained by default on a first logic value. As recited in independent Claim 20, for example, the method includes providing each device with the ability to tie the clock line to a potential representing a second logic value opposite the first logic value, and tying the clock line to the second logic value, via the two devices, when data is transmitted. The method further includes maintaining the tie to the clock line by the device to which the data is sent while the device has not read the data, and maintaining the data on the data line by the device sending the data at least until an instant when the clock line is released by the device to which the data is sent.

Independent Claim 32 is directed to a similar method, independent Claims 44 and 46 are directed to related data transmitting/receiving devices, independent Claim 48 is directed to a related synchronous data transmission system, and independent Claim 51 is directed to a related communication interface circuit.

II. The Claims Are Patentable

The Examiner rejected independent Claims 20, 32, 44, 46, 48, and 51 based upon the I^2C Bus Specification, Version 2.1 (the "Specification"). The Examiner notes that an I^2C bus includes a data line SDA and a clock line SCL. The Examiner points to FIG. 5 on page 9 of the specification and further to section 7.1 on page 10, which states that "[i]f a slave can't receive or transmit another complete byte of data until it has performed some other function, for example servicing an internal interrupt, it can hold the clock line SCL LOW to force the master into a wait state." The Examiner therefore contends that the Specification teaches all of the recitations of the above-noted independent claims.

It is respectfully submitted that the Examiner mischaracterizes the Specification, as this reference does not teach or fairly suggest that the master and slave devices each has the ability to tie the clock line to a potential representing a second logic value different than a first logic value, and then tying the clock line to the second logic value via the two devices when data is transmitted. More particularly, referring to FIG. 6 of the Specification, which is reproduced below for the Examiner's convenience, after the data transmission is initiated by the START condition, the master device sends a series of eight clock pulses 1, 2, 3, …, 8 on the clock line SCL along with one acknowledge pulse 9, while the slave device is "silent" (i.e., it does not pull the clock line down). Since the clock pulses are generated using the open-drain method (i.e., the clock line SCL

is pulled-up by a passive component as a resistor and the master pulls it down to generate a pulse), the slave device cannot pull the line down at the same time the master device is sending clock pulses. Otherwise, there would be no clock pulses.

Moreover, the I2C master device cannot pull the clock line down to emit the START condition as long it is pulled down by the slave device. As noted on page 9 of the Specification, "[b]us clock signals from a master can only be altered when they are stretched by a slow-slave device holding-down the clock line, or by another master when arbitration occurs." Moreover, this fact is also demonstrated by the above-quoted text from section 7.1 of the Specification noted by the Examiner. That is, the above-quoted text is saying that as long as the slave device holds the clock line down, the master cannot alternatively pull the clock line down then release it to send the clock signal.

Accordingly, the Specification simply fails to teach or fairly suggest all of the recitations of independent Claims 20, 32, 44, 46, 48, and 51. Thus, it is submitted that these claims are patentable over the prior art. Their respective dependent claims, which recite yet further distinguishing features, are also patentable over the prior art and require no further discussion herein.

CONCLUSIONS

In view of the foregoing, it is submitted that all of the claims are patentable. Accordingly, a Notice of Allowance is respectfully requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to

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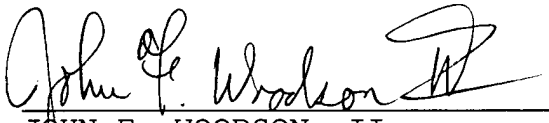
contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,



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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 17th day of February, 2006.